# APPARATUS OF A DIGITAL ECHO CANCELLER AND METHOD THEREFOR

## CROSS-REFERENCE TO RELATED APPLICATION

This application claims the priority benefit of Taiwan application serial no. 89126182, filed Dec.8, 2000.

## BACKGROUND OF THE INVENTION

### Field of Invention

The present invention relates generally to a method and apparatus of a digital echo canceller. More particularly, the present invention relates to a method and apparatus of a digital echo canceller that only responds to echo signals to perform a multiplication-and-addition function.

### Description of the Related Art

Fig. 1 illustrates a performance of a full-duplex digital transceiver. Both ends of the full-duplex digital transceiver are connected to a cable 22. Each end of the full-duplex digital transceiver has a transceiver 18 or 20. The transceiver 18 at the left end of the full-duplex digital transceiver comprises a transmitter (TX) 12, a receiver (RX) 14 and a hybrid circuit 16. The transmitter 12 and the receiver 14 are connected to the hybrid circuit 16 to receive and transmit signals.

If the transceiver 18 at the left end of the full-duplex digital transceiver is used as a near-end transceiver, the other transceiver at the right end will be a far-end transceiver. When the transmitter 12 transmits a signal to the far-end of the full-duplex digital

transceiver 20, the transmitter will often not match the impedance of the far-end full-duplex digital transceiver 20 due to a transmitting cable 22. A far-end echo signal that will transmit to the near-end of the full-duplex digital transceiver 16 influences the received signal of the receiver 14. An interfering noise will occur.

To prevent the above-mentioned state from occurring, the conventional method will require designing a canceller to eliminate the echo signals. The structure illustrated in Fig.2 is an adaptive finite impulse response digital echo canceller (adaptive FIR digital echo canceller). Xn signals are transmitted to a plurality of delay circuits D. After receiving the Xn signals, an output of each delay circuit D produces a signal. These signals are multiplied respectively to a plurality of significant coefficients $C_0, C_1, C_2, \ldots\ldots C_{N-2}, C_{N-1}$ to produce multiplied values. These multiplied values are then added together to produce a sum (the sum $\sum$ is shown on the Fig.2). An estimated echo signal is thus produced to eliminate the interference noise.

The above mentioned structure transmits signals utilizing a longer transmitting cable and a higher frequency (for example, a gigabit ethernet case, at the sample rate of 125 Mhz) to produce an echo signal's length that is shown in Fig. 3. The length of the echo signal is approximately 80 EC taps long. When the length of the echo signal is longer, the number of significant coefficients $C_0, C_1 \ldots . C_{N-2}, C_{N-1}$ that multiply respectively to the signals transmitted by the delay circuits D of Fig. 2 will increase. As a result, the amount of addition and multiplication operations that have to be calculated will also increase. The whole operation is not only complex, but the cost of the hardware is also high.

## SUMMARY OF THE INVENTION

According to above, the present invention provides an installation of a digital echo

canceller and method therefor. It is an object of the present invention to perform a multiplication-and-addition functions according to an echo part that relates to an echo signal so that an unnecessary circuit design can be omitted.

The present invention provides an installation of a digital echo canceller. The digital echo canceller is suitable for a full-duplex digital transceiver to eliminate an echo signal that is produced by the full-duplex digital transceiver.

The receiver of the full-duplex digital transceiver is connected to a first receiving end and a second receiving end by a cable. The first receiving end produces an input signal.

The structure of the present invention comprises a plurality of first-set delay circuits, a selector, a plurality of second-set delay circuits, a plurality of multipliers and an adder. The plurality of first-set delay circuits comprise an input and an output, wherein the input and the output are connected in series. An input signal that is received by a first input is transmitted out from the full-duplex digital transceiver. First-set delay circuits are arranged into groups, and each group has N delay circuits. The selector comprises an input and an output. The input of the selector is according to an exhaustive search to select any set of delay circuits' outputs for connection. A plurality of second-set delay circuits comprise an input and output, wherein the input and the output are connected in series. The first input is connected to the output of the selector. The number of the multipliers is the same as the number of the second-set of the delay circuits. The multipliers are connected respectively to each output of the second-set delay circuits. Each of these multipliers are multiplied respectively to an EC coefficient to produce signals. An adder will receive all these signals that are produced from the multipliers and add these values together to produce a sum, wherein the sum is an

estimated echo signal that will cancel the echo signal.

The exhaustive search function is according to the energy sum that is produced by each set of delay circuits. The largest energy sum of the delay circuits' set is selected to connect its output to the selector. The energy sum can be calculated by a formula $E(s)=\sum_{i=1}^{N_s} ci^2(s)$, wherein E(s) is the EC energy sum, Ci(s) is the EC coefficient and $N_s$ is the response number of the echo signal and the $N_s$ number is same as the number of the second-set of delay circuits. The response number is 20 for example.

It is one object of the present invention to provide a method of a digital echo canceller to cancel an echo signal. This method is suitable for a full-duplex digital transceiver. A first receiving end is connected to a second receiving end by a cable. The input signal is transmitted by the first receiving end.

In order to determine the significant part of echo signals, the searching steps comprise: (a) the total number of search S can be calculated from an equation $S=N_{is,\max}/\Delta N$, wherein the largest response number of the insignificant part of the response signal is $N_{is,\max}$, and $\Delta N$ is an incremental number. $N_{is,\max}$ is found first; then the value $\Delta N$ is determined from the value of $N_{is,\max}$. Once these two values are known, the total number of searching S can be calculated.

(b) an equation $N_{is}(s)=s*\Delta N$ is used to search for a starting point of the echo response, wherein $\Delta N$ is assumed to be 10 and the value of s starts from 0. Once the starting point of the echo response $N_{is}(s)$ is found, the response number of searching $N_s$ can be determined. The $N_s$ value is used to calculate the energy sum of EC from an

energy equation $E(s) = \sum_{i=1}^{N_s} ci^2(s)$, wherein E(s) is the energy sum of EC, and Ci(s) is the EC coefficient.

(c) the value of S that is calculated in step (a) is used as a reference to determine the value of s. In order to get s = S, the calculation process has to repeat step (b) until s = S and $N_{is}(s) = N_{is,\max}$.

(d), the largest energy sum that is calculated during each searching is chosen for the significant part.

(e), finally the values of the significant part are multiplied to corresponding correlation coefficients. The results of this multiplication operation are then added together to give an estimated echo signal that will cancel the echo signal. From the above-mentioned, the value of $\Delta N$ is set at 10, and the value of $N_s$ is set at 20, for example.

It is to be understood that both the forgoing general description and the following detailed description are exemplary, and are intended to provide further explanation of the invention as claimed.

## BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings are included to provide a further understanding of the present invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention. In the drawings,

Fig. 1 is a diagram that illustrates a performance of a full-duplex digital transceiver;

Fig. 2 is a diagram that illustrates a structure of an adaptive FIR digital echo

canceller;

Fig. 3 is a graph of the distribution of the echo signal;

Fig. 4 is a diagram that illustrates an apparatus of a digital echo canceller according to a preferred embodiment of the present invention.

## DESCRIPTION OF THE PREFERRED EMBODIMENTS

The conventional structure of a digital echo canceller utilizes a longer transmitting cable and a higher frequency; therefore, the amount of multiplication and addition operations between the significant coefficients and the signals that are produced by the delay circuits increases. As a result the whole operation becomes complex and the cost of the hardware increases.

According to the above-mentioned disadvantage, a method can be obtained from Fig. 3 to improve the conventional structure. Fig. 3 illustrates a graph of the echo signal distribution. According to the average calculation, the values of 10 cycles are normally used but in order to reduce the deviation, an extra 10 cycles (from the first part and the last part) are taken into account for the calculation. The results that we obtained from the calculation can be divided into two parts, wherein the front part is an insignificant part and the latter part is a significant part.

The method of the present invention of a digital echo canceller is to connect from a first receiving end of the full-duplex digital transceiver to its second receiving end by using a cable. The steps of this connecting process comprise :

(a) $N_{is,\max}$ is the largest response number of the insignificant part of the response signal that shows in Fig. 3 of the insignificant part of echo signals, we will therefore set the value of $N_{is,\max}$ at 60. $\Delta N$ is an incremental number, wherein we set the value at

10 ,for example. The total number of search S can be calculated from an equation $S=N_{is,\max}/\Delta N$, S = 60/10 = 6.

(b) an equation $N_{is}(s) = s * \Delta N$ is used to search for a starting point of the echo response, wherein $\Delta N$ is set to be 10 and the value of s starts from 0. Once the starting point of the echo response $N_{is}(s)$ is found, the response number of searching $N_s$ can be determined. From Fig. 3, we use 10 cycles of the echo signal distribution, but in order to have a more acutely value an extra 10 cycles are taken from the first part and the last part of the distribution. Therefore, the $N_s$ value is set at 20. The $N_s$ value is used to calculate the energy sum of EC from an energy equation $E(s) = \sum_{i=1}^{N_s} ci^2(s)$, wherein E(s) is the energy sum of EC, and Ci(s) is the EC coefficient. In general, in the insignificant part of the echo signal distribution, the value of Ci(s) is usually very small, and the E(s) that is calculated is almost 0. The E(s) value starts to become larger when the echo signal distributes at the significant part.

(c) the value of S that is calculated in step (a) is used as a reference to determine the value of s. In order to get s = S, the calculation process has to repeat step (b) until s = S and $N_{is}(s) = N_{is,\max}$. The total number of searching is S+1, and each energy sum E(s) is calculated.

(d) the largest energy sum that is calculated during each searching is selected for the significant part.

(e) the selected values of the significant part are multiplied to corresponding correlation coefficients. The results of this multiplication operation are then added together to give an estimated echo signal that will cancel the echo signal.

Fig. 4 is a diagram that illustrates an apparatus of a digital echo canceller according to a preferred embodiment of the present invention. The digital echo canceller that is suitable for a full-duplex digital transceiver (shown in Fig 1) is used to cancel the echo signal.

The canceller comprises a plurality of first- set delay circuits 40, a selector 42, a plurality of second set delay circuits 44, a plurality of multipliers 46 and a adder 48. The plurality of first-set delay circuits 40, each has an input and an output and are connected in series. The first input receives an input signal that is transmitted by the full-duplex digital transceiver (Ref. Fig 1). The first-set delay circuits are arranged in groups and each group has N delay circuits. Fig 4 shows the first group of the first-set delay circuits 50 is from number 1 to number $\Delta N$, and second group 52 is from $\Delta N + 1$ to $2\Delta N$.

The input of the selector 42 is used for searching and it selects to connect any one of the output of the first-set delay circuits. The searching function depends on the plurality of energy sums are produced from the first-set delay circuits (for example 50 and 52 in Fig 4), the energy equation is $E(s) = \sum_{i=1}^{N_s} ci^2(s)$, wherein E(s) is the energy sum of EC, and Ci(s) is the EC coefficient. $N_s$ is the response number of the echo signal and the number of $N_s$ is the same as the number of second-set of delay circuits, and the number of $N_s$ is set at 20 ,for example.

The first-set delay circuits can be designed into a simple circuit (not shown in the diagram). The selector will the select the largest energy sum of an output of the first-set delay circuits to use for the significant part, and the selected output of the delay circuit is connected to the input of the selector 42.

The second-set delay circuits 44 are connected in series. The output of the selector

42 is connected to the input of the second-set delay circuits. The multipliers 46 have the same number as the second-set circuits 44. A plurality of correlation coefficients will be received by the multipliers when the signals are produced from the outputs of the second-set circuits. These signals are multiplied respectively to the correlation coefficients. The results are the added together by a adder to produce an estimated echo signal (ESS). The estimated echo signal is used to cancel the echo signal.

According to above, the present invention provides an apparatus of a digital echo canceller and method therefor. It is an object of the present invention to perform a multiplication-and-addition functions according to an echo part that relates to an echo signal so that an unnecessary circuit design can be omitted. The cost of the hardware can be reduced.

Other embodiments of the invention will appear to those skilled in the art from consideration of the specification and practice of the invention disclosed herein. It is intended that the specification and examples be considered as exemplary only, with a true scope and spirit of the invention being indicated by the following claims.